



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/665,757 | 09/19/2003 | Glenn J. Leedy | ELM-1 CONT. 9 | 6828 |

7590

06/26/2006

PHILIP R POH
FISH & NEAVE
1251 AVENUE OF THE AMERICAS
NEW YORK, NY 10020-1105

EXAMINER

PERKINS, PAMELA E

ART UNIT PAPER NUMBER

2822

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/665,757

Applicant(s)

LEEDY, GLENN J.

Examiner

Pamela E. Perkins

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) See Continuation Sheet is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 156-291, 394-399, 409-424, 448-455, 457, 460, 462-464, 466-468, 470-485 and 523-530 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>5/19/06, 5/26/06</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is in response to the filing of the RCE on 26 May 2006. Claims 156-291, 394-399, 409-424, 448-455, 457, 460, 462-464, 466-468, 470-485 and 523-530 are pending.

The indicated allowability of claims 156-291, 394-399, 409-424, 448-455, 457, 460, 462-464, 466-468, 470-485 and 523-530 is withdrawn in view of the newly discovered reference(s) to the material used to form the dielectric layers. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 156, 157, 160, 161, 164, 165, 167, 169, 172-175, 177, 220, 222-225, 229-234, 236-241, 245-252, 268, 271, 274, 286, 289, 394, 395, 397-399, 409-412, 419-424, 451, 474, 479 and 484 are rejected under 35 U.S.C. 102(b) as being anticipated by Findler et al. (5,071,510).

Referring to claims 156, 157, 160, 165, 167, 169, 172, 175, 177, 220, 223, 229, 232, 234, 236, 239, 245, 248, 268, 271, 274, 286, 289, 451, 474, 479 and 484, Findler et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; forming circuitry having active devices at least one of in and on the

Art Unit: 2822

principal surface of the substrate (1); depositing a silicon nitride dielectric membrane/layer (6) as part of the circuitry; and removing a major portion the substrate (1) throughout a full extent thereof without impairing the structural integrity of the integrated circuit (Fig. 1; col. 5, lines 5-33). Although Findler et al. do not specifically disclose the silicon nitride dielectric layer as a stress-controlled dielectric membrane/layer, it is inherently so because applicant's stress-controlled dielectric membrane/layer is silicon nitride. Therefore the silicon nitride dielectric layer disclosed in Findler et al. is capable of forming at least one of flexible membrane, an elastic membrane, and a free standing membrane.

Claims 161, 173, 233, 237 and 249. Depositing the at least one of the silicon nitride dielectric films using Plasma Enhanced Chemical Vapor Deposition (col. 6, lines 13-17).

Claims 164, 174, 222, 238 and 250. Wherein the substrate is a silicon wafer (abstract).

Claims 224, 230, 240, 246 and 251. Wherein the major portion of the substrate is removed prior to forming the circuitry (col. 7, lines 13-21).

Claims 225, 231, 241, 247 and 252. Wherein the major portion of the substrate is removed after forming the circuitry (col. 7, lines 13-21).

Claims 394, 395 and 397-399. Forming a barrier layer (2) in the substrate (1) parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer (2) (col. 5, lines 15-20).

Claims 409, 411, 419, 421 and 423. Wherein the at least one or more stress-controlled dielectric layers are formed from an inorganic dielectric material (col. 5, lines 29-33).

Art Unit: 2822

Claims 410, 412, 420, 422 and 424. Wherein at least a major portion of the inorganic dielectric material is formed from a nitride of silicon (col. 5, lines 29-33).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 158, 159, 162, 163, 170, 171, 227, 228, 243, 244, 254, 255, 267, 269, 275, 287, 290, 452, 457, 475, 480 and 485 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findler et al. in view of Hori et al. (5,188,706).

Findler et al. disclose the subject matter claimed above except the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm².

Hori et al. disclose a method of lithographic pattern generation where an array of exposure cells is provided on a substrate, wherein the exposure cells expose separate areas of a surface to be exposed; and providing at least one stress-controlled dielectric layer on the substrate (col. 1, lines 9-13; col. 4, lines 5-59).

Referring to claims 158, 162, 170, 227, 243, 254, 267, 269, 272, 275, 287 and 290, Hori et al. disclose the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm² (col. 8, lines 32-59).

Referring to claim 159, 163, 171, 228, 244, 255, 267, 269, 272, 275, 287 and 290, Hori et al. disclose the stress as tensile (col. 8, lines 32-59).

Art Unit: 2822

Since Findler et al. and Hori et al. are both from the same field of endeavor, a method of lithographic pattern generation, the purpose disclosed by Hori et al. would have been recognized in the pertinent art of Findler et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. by the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm² as taught by Hori et al. to increase density and stress stability (col. 4, lines 5-8).

Referring to claims 452, 457, 475, 480 and 485 Findler et al. do not disclose forming the elastic low stress/stress-controlled dielectric membrane/layer at a temperature of about 400°C. It would have been obvious to one having ordinary skill in the art at the time invention was made to forming the elastic low stress/stress-controlled dielectric membrane/layer at a temperature of about 400°C disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Claims 166, 168, 176, 178, 186, 188, 221, 226, 235, 242, 253, 298, 300, 336, 338, 345, 352, and 366 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findler et al. in view of Shimizu et al. (4,618,397).

Findler et al. disclose the subject matter claimed above except the integrated circuit being able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

Shimizu et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; and forming circuit devices/circuitry/active devices (4) on the principal surface (col. 1, lines 29-44).

Referring to claims 166, 168, 176, 178, 186, 188, 221, 226, 235, 242, 253, 298, 300, 336, 338, 345, 352 and 366, Shimizu et al. disclose the integrated circuit being able to be thinned to about 25 microns throughout a full extent thereof while retaining its structural integrity (col. 1, lines 45-56).

Since Findler et al. and Shimizu et al. are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Shimizu et al. would have been recognized in the pertinent art of Findler et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. by the integrated circuit being able to be thinned to about 25 microns throughout a full extent thereof while retaining its structural integrity as taught by to prevent defects (col. 1, lines 38-44).

Claims 179, 182-185, 187, 189, 192-194, 196, 207-214, 256-261, 265, 266, 277, 396, 413, 414, 415, 416, 448, 453, 458, 471, 476 and 481 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findler et al. in view of Stein (4,070,230).

Findler et al. disclose the subject matter claimed above except transferring information through the interconnections formed passing through the stress-controlled dielectric layer.

Referring to claims 179, 182, 185, 187, 189, 192, 194, 196, 207-214, 256-261, 265, 266, 277, 280, 448,453, 458, 462, 466, 471, 476 and 481, Stein discloses a method of making an integrated circuit where a substrate (1) has a principal surface; forming circuit devices/circuitry/active devices (8) on the principal surface; and forming a layer (9) overlying the circuit devices (8) (col. 4, lines 27-55). Stein further discloses the integrated circuit able to have a major portion of the substrate (1) removed throughout a full extent thereof while retaining its structural integrity (col. 5, lines 7-24). Stein also discloses transferring information through interconnections formed passing through the layer, wherein the interconnections are at least one of electrical and optical interconnections (col. 5, lines 32-41).

Since Findler et al. and Stein are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Stein would have been recognized in the pertinent art of Findler et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. by transferring information through interconnections formed passing through the layer as taught by Stein to prevent defects (col. 1, lines 22-48).

Referring to claims 183 and 193, Findler et al. disclose depositing the at least one of the silicon nitride dielectric films using Plasma Enhanced Chemical Vapor Deposition (col. 6, lines 13-17).

Referring to claim 184, Findler et al. disclose wherein the substrate is a silicon wafer (abstract).

Referring to claims 277 and 280, although Findler et al. do not specifically disclose the silicon nitride dielectric layer as a stress-controlled dielectric membrane/layer, it is inherently so because applicant's stress-controlled dielectric membrane/layer is silicon nitride. Therefore the silicon nitride dielectric layer disclosed in Findler et al. is capable of forming at least one of flexible membrane, an elastic membrane, and a free standing membrane.

Referring to claim 396, Findler et al disclose forming a barrier layer (2) in the substrate (1) parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer (2) (col. 5, lines 15-20).

Referring to claims 413 and 415, Findler et al. disclose wherein the at least one or more stress-controlled dielectric layers are formed from an inorganic dielectric material (col. 5, lines 29-33).

Referring to claims 414 and 416, Findler et al. disclose wherein at least a major portion of the inorganic dielectric material is formed from a nitride of silicon (col. 5, lines 29-33).

Referring to claims 462 and 466, Findler et al. do not disclose forming the elastic low stress/stress-controlled dielectric membrane/layer at a temperature of about 400°C. It would have been obvious to one having ordinary skill in the art at the time invention was made to forming the elastic low stress/stress-controlled dielectric membrane/layer at a temperature of about 400°C disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art,

Art Unit: 2822

discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Claims 180, 181, 190, 191, 278, 281 and 284 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findler et al. in view of Stein as applied to claims 179 and 189 above, and further in view of Hori et al.

Findler et al. in view of Stein disclose the subject matter claimed above except the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm².

Hori et al. disclose a method of lithographic pattern generation where an array of exposure cells is provided on a substrate, wherein the exposure cells expose separate areas of a surface to be exposed; and providing at least one stress-controlled dielectric layer on the substrate (col. 1, lines 9-13; col. 4, lines 5-59).

Referring to claims 180, 190, 278, 281 and 284, Hori et al. disclose the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm² (col. 8, lines 32-59).

Referring to claims 181, 191, 278, 281 and 284, Hori et al. disclose the stress as tensile (col. 8, lines 32-59).

Since Findler et al. and Hori et al. are both from the same field of endeavor, a method of lithographic pattern generation, the purpose disclosed by Hori et al. would have been recognized in the pertinent art of Findler et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. by the stress of the stress-controlled dielectric layer is less than about $8 \times$

10^8 dynes/cm² as taught by Hori et al. to increase density and stress stability (col. 4, lines 5-8).

Claims 186, 188, 195 and 197 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findler et al. in view of Stein as applied to claim 179 and 189 above, and further in view of Shimizu et al.

Findler et al. in view of Stein disclose the subject matter claimed above except the integrated circuit being able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

Shimizu et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; and forming circuit devices/circuitry/active devices (4) on the principal surface (col. 1, lines 29-44).

Referring to claims 186, 188, 195 and 197, Shimizu et al. disclose the integrated circuit being able to be thinned to about 25 microns throughout a full extent thereof while retaining its structural integrity (col. 1, lines 45-56).

Since Findler et al. and Shimizu et al. are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Shimizu et al. would have been recognized in the pertinent art of Findler et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. by the integrated circuit being able to be thinned to about 25 microns throughout a full extent thereof while retaining its structural integrity as taught by to prevent defects (col. 1, lines 38-44).

Claims 198, 201-203, 205, 283, 417, 418 and 470 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findler et al. in view of Bergmans et al. (4,835,765).

Findler et al. disclose the subject matter claimed above except an integrated circuit having a data source formed on a first portion of the integrated circuit, a data sink formed on a second portion of the integrated circuit, and transferring a plurality of data bytes between the data source and data sink of an interconnect circuitry of the integrated circuit.

Referring to claim 198, Bergmans et al. disclose a method of using an integrated circuit having a data source (7) formed on a first portion of the integrated circuit (1), a data sink (13) formed on a second portion of the integrated circuit (1), interconnect circuitry interconnecting the data source (7) and the data sink (13); transferring a plurality of data bytes between the data source (7) and data sink (13) of the interconnect circuitry of the integrated circuit (1) (col. 3, lines 30-51).

Since Findler et al. and Bergmans et al. are both from the same field of endeavor, a method of using an integrated circuit, the purpose disclosed by Bergmans et al. '663 would have been recognized in the pertinent art of Findler et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. by having an integrated circuit having a data source formed on a first portion of the integrated circuit, a data sink formed on a second portion of the integrated circuit, and transferring a plurality of data bytes between the data source and data sink of an interconnect circuitry of the integrated circuit as taught by Bergmans et al. to reduce defects (col. 3, lines 52-64).

Referring to claim 201, Findler et al. disclose depositing at least one silicon nitride dielectric membrane/layer (6) (col. 5, lines 5-33).

Referring to claims 202, Findler et al. disclose depositing the at least one of the silicon nitride dielectric films using Plasma Enhanced Chemical Vapor Deposition (col. 6, lines 13-17).

Referring to claims 203 and 205, Findler et al. disclose removing a major portion the substrate (1) throughout a full extent thereof without impairing the structural integrity of the integrated circuit (Fig. 1; col. 5, lines 5-33).

Referring to claim 283, although Findler et al. do not specifically disclose the silicon nitride dielectric layer as a stress-controlled dielectric membrane/layer, it is inherently so because applicant's stress-controlled dielectric membrane/layer is silicon nitride. Therefore the silicon nitride dielectric layer disclosed in Findler et al. is capable of forming at least one of flexible membrane, an elastic membrane, and a free standing membrane.

Referring to claim 417, Findler et al. disclose wherein the at least one or more stress-controlled dielectric layers are formed from an inorganic dielectric material (col. 5, lines 29-33).

Referring to claim 418, Findler et al. disclose wherein at least a major portion of the inorganic dielectric material is formed from a nitride of silicon (col. 5, lines 29-33).

Referring to claim 470, Findler et al. do not disclose forming the elastic low stress/stress-controlled dielectric membrane/layer at a temperature of about 400°C. It would have been obvious to one having ordinary skill in the art at the time invention was

Art Unit: 2822

made to forming the elastic low stress/stress-controlled dielectric membrane/layer at a temperature of about 400°C disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Claims 199 and 200 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findler et al. in view of Bergmans et al. as applied to claims 179 and 189 above, and further in view of Hori et al.

Findler et al. in view of Bergmans et al. disclose the subject matter claimed above except the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm².

Hori et al. disclose a method of making an integrated circuit where at least one stress-controlled dielectric layer is formed on a substrate (col. 1, lines 9-13; col. 4, lines 5-59).

Referring to claim 199, Hori et al. disclose the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm² (col. 8, lines 32-59).

Referring to claim 200, Hori et al. disclose the stress as tensile (col. 8, lines 32-59).

Since Findler et al. and Hori et al. are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Hori et al. would have been recognized in the pertinent art of Findler et al. Therefore, it would have been

Art Unit: 2822

obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. by the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm² as taught by Hori et al. to increase density and stress stability (col. 4, lines 5-8).

Claims 204 and 206 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findler et al. in view of Bergmans et al. as applied to claim 179 and 189 above, and further in view of Shimizu et al.

Findler et al. in view of Bergmans et al. disclose the subject matter claimed above except the integrated circuit being able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

Shimizu et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; and forming circuit devices/circuitry/active devices (4) on the principal surface (col. 1, lines 29-44).

Referring to claims 204 and 206, Shimizu et al. disclose the integrated circuit being able to be thinned to about 25 microns throughout a full extent thereof while retaining its structural integrity (col. 1, lines 45-56).

Since Findler et al. and Shimizu et al. are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Shimizu et al. would have been recognized in the pertinent art of Findler et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. by the integrated circuit being able to be thinned to about 25 microns

throughout a full extent thereof while retaining its structural integrity as taught by to prevent defects (col. 1, lines 38-44).

Claims 215, 216, 262-264, 270, 273, 276, 288, 291, 523, 524 and 528-530 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findley et al. in view of Hori et al. and Shimizu et al.

Findler et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; forming circuitry having active devices at least one of in and on the principal surface of the substrate (1); depositing a silicon nitride dielectric membrane/layer (6) as part of the circuitry; and removing a major portion the substrate (1) throughout a full extent thereof without impairing the structural integrity of the integrated circuit (Fig. 1; col. 5, lines 5-33). Findler et al. further disclose depositing the at least one of the silicon nitride dielectric films using Plasma Enhanced Chemical Vapor Deposition (col. 6, lines 13-17) and wherein the substrate is a silicon wafer (abstract). Findler et al. also disclose the at least one or more stress-controlled dielectric layers are formed from an inorganic dielectric material (col. 5, lines 29-33), wherein at least a major portion of the inorganic dielectric material is formed from a nitride of silicon (col. 5, lines 29-33).

Although Findler et al. do not specifically disclose the silicon nitride dielectric layer as a stress-controlled dielectric membrane/layer, it is inherently so because applicant's stress-controlled dielectric membrane/layer is silicon nitride. Therefore the

Art Unit: 2822

silicon nitride dielectric layer disclosed in Findler et al. is capable of forming at least one of flexible membrane, an elastic membrane, and a free standing membrane.

Findler et al. do not disclose stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm².

Hori et al. disclose a method of lithographic pattern generation where an array of exposure cells is provided on a substrate, wherein the exposure cells expose separate areas of a surface to be exposed; and providing at least one stress-controlled dielectric layer on the substrate (col. 1, lines 9-13; col. 4, lines 5-59). Hori et al. further disclose the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm² (col. 8, lines 32-59). Hori et al. also disclose the stress as tensile (col. 8, lines 32-59).

Since Findler et al. and Hori et al. are both from the same field of endeavor, a method of lithographic pattern generation, the purpose disclosed by Hori et al. would have been recognized in the pertinent art of Findler et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. by the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm² as taught by Hori et al. to increase density and stress stability (col. 4, lines 5-8).

Findler et al. in view of Hori et al. do not disclose the integrated circuit being able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

Shimizu et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; and forming circuit devices/circuitry/active devices

Art Unit: 2822

(4) on the principal surface (col. 1, lines 29-44). Shimizu et al. further disclose the integrated circuit being able to be thinned to about 25 microns throughout a full extent thereof while retaining its structural integrity (col. 1, lines 45-56).

Since Findler et al., Hori et al. and Shimizu et al. are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Shimizu et al. would have been recognized in the pertinent art of Findler et al. and Hori et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. and Hori et al. by the integrated circuit being able to be thinned to about 25 microns throughout a full extent thereof while retaining its structural integrity as taught by to prevent defects (col. 1, lines 38-44).

Claims 217, 218, 279, 282, 525 and 526 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findler et al. in view of Stein as applied to claims 179 and 189 above, and further in view of Hori et al. and Shimizu et al.

Findler et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; forming circuitry having active devices at least one of in and on the principal surface of the substrate (1); depositing a silicon nitride dielectric membrane/layer (6) as part of the circuitry; and removing a major portion the substrate (1) throughout a full extent thereof without impairing the structural integrity of the integrated circuit (Fig. 1; col. 5, lines 5-33). Findler et al. further disclose depositing the at least one of the silicon nitride dielectric films using Plasma Enhanced Chemical Vapor Deposition (col. 6, lines 13-17) and wherein the substrate is a silicon wafer

Art Unit: 2822

(abstract). Findler et al. also disclose the at least one or more stress-controlled dielectric layers are formed from an inorganic dielectric material (col. 5, lines 29-33), wherein at least a major portion of the inorganic dielectric material is formed from a nitride of silicon (col. 5, lines 29-33).

Although Findler et al. do not specifically disclose the silicon nitride dielectric layer as a stress-controlled dielectric membrane/layer, it is inherently so because applicant's stress-controlled dielectric membrane/layer is silicon nitride. Therefore the silicon nitride dielectric layer disclosed in Findler et al. is capable of forming at least one of flexible membrane, an elastic membrane, and a free standing membrane.

Findler et al. do not disclose transferring information through the interconnections formed passing through the stress-controlled dielectric layer.

Stein discloses a method of making an integrated circuit where a substrate (1) has a principal surface; forming circuit devices/circuitry/active devices (8) on the principal surface; and forming a layer (9) overlying the circuit devices (8) (col. 4, lines 27-55). Stein further discloses the integrated circuit able to have a major portion of the substrate (1) removed throughout a full extent thereof while retaining its structural integrity (col. 5, lines 7-24). Stein also discloses transferring information through interconnections formed passing through the layer, wherein the interconnections are at least one of electrical and optical interconnections (col. 5, lines 32-41).

Since Findler et al. and Stein are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Stein would have been recognized in the pertinent art of Findler et al. Therefore, it would have been obvious to

Art Unit: 2822

one of ordinary skill in the art at the time the invention was made to modify Findler et al. by transferring information through interconnections formed passing through the layer as taught by Stein to prevent defects (col. 1, lines 22-48).

Findler et al. in view of Stein do not disclose stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm².

Hori et al. disclose a method of lithographic pattern generation where an array of exposure cells is provided on a substrate, wherein the exposure cells expose separate areas of a surface to be exposed; and providing at least one stress-controlled dielectric layer on the substrate (col. 1, lines 9-13; col. 4, lines 5-59). Hori et al. further disclose the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm² (col. 8, lines 32-59). Hori et al. also disclose the stress as tensile (col. 8, lines 32-59).

Since Findler et al., Stein and Hori et al. are both from the same field of endeavor, a method of lithographic pattern generation, the purpose disclosed by Hori et al. would have been recognized in the pertinent art of Findler et al. and Stein. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. and Stein by the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm² as taught by Hori et al. to increase density and stress stability (col. 4, lines 5-8).

Findler et al. in view of Stein do not disclose the integrated circuit being able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

Shimizu et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; and forming circuit devices/circuitry/active devices (4) on the principal surface (col. 1, lines 29-44). Shimizu et al. further disclose the integrated circuit being able to be thinned to about 25 microns throughout a full extent thereof while retaining its structural integrity (col. 1, lines 45-56).

Since Findler et al., Stein and Shimizu et al. are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Shimizu et al. would have been recognized in the pertinent art of Findler et al. and Stein. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. and Stein by the integrated circuit being able to be thinned to about 25 microns throughout a full extent thereof while retaining its structural integrity as taught by to prevent defects (col. 1, lines 38-44).

Claims 219, 285 and 527 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findler et al. in view of Bergmans et al. as applied to claim 198 above, and further in view of Stein, Hori et al. and Shimizu et al.

Findler et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; forming circuitry having active devices at least one of in and on the principal surface of the substrate (1); depositing a silicon nitride dielectric membrane/layer (6) as part of the circuitry; and removing a major portion the substrate (1) throughout a full extent thereof without impairing the structural integrity of the integrated circuit (Fig. 1; col. 5, lines 5-33). Findler et al. further disclose depositing the

Art Unit: 2822

at least one of the silicon nitride dielectric films using Plasma Enhanced Chemical Vapor Deposition (col. 6, lines 13-17) and wherein the substrate is a silicon wafer (abstract). Findler et al. also disclose the at least one or more stress-controlled dielectric layers are formed from an inorganic dielectric material (col. 5, lines 29-33), wherein at least a major portion of the inorganic dielectric material is formed from a nitride of silicon (col. 5, lines 29-33).

Although Findler et al. do not specifically disclose the silicon nitride dielectric layer as a stress-controlled dielectric membrane/layer, it is inherently so because applicant's stress-controlled dielectric membrane/layer is silicon nitride. Therefore the silicon nitride dielectric layer disclosed in Findler et al. is capable of forming at least one of flexible membrane, an elastic membrane, and a free standing membrane.

Findler et al. disclose the subject matter claimed above except an integrated circuit having a data source formed on a first portion of the integrated circuit, a data sink formed on a second portion of the integrated circuit, and transferring a plurality of data bytes between the data source and data sink of an interconnect circuitry of the integrated circuit.

Bergmans et al. disclose a method of using an integrated circuit having a data source (7) formed on a first portion of the integrated circuit (1), a data sink (13) formed on a second portion of the integrated circuit (1), interconnect circuitry interconnecting the data source (7) and the data sink (13); transferring a plurality of data bytes between the data source (7) and data sink (13) of the interconnect circuitry of the integrated circuit (1) (col. 3, lines 30-51).

Since Findler et al. and Bergmans et al. are both from the same field of endeavor, a method of using an integrated circuit, the purpose disclosed by Bergmans et al. '663 would have been recognized in the pertinent art of Findler et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. by having an integrated circuit having a data source formed on a first portion of the integrated circuit, a data sink formed on a second portion of the integrated circuit, and transferring a plurality of data bytes between the data source and data sink of an interconnect circuitry of the integrated circuit as taught by Bergmans et al. to reduce defects (col. 3, lines 52-64).

Findler et al. in view of Bergmans et al. do not disclose transferring information through the interconnections formed passing through the stress-controlled dielectric layer.

Stein discloses a method of making an integrated circuit where a substrate (1) has a principal surface; forming circuit devices/circuitry/active devices (8) on the principal surface; and forming a layer (9) overlying the circuit devices (8) (col. 4, lines 27-55). Stein further discloses the integrated circuit able to have a major portion of the substrate (1) removed throughout a full extent thereof while retaining its structural integrity (col. 5, lines 7-24). Stein also discloses transferring information through interconnections formed passing through the layer, wherein the interconnections are at least one of electrical and optical interconnections (col. 5, lines 32-41).

Since Findler et al., Bergmans et al. and Stein are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Stein

Art Unit: 2822

would have been recognized in the pertinent art of Findler et al. and Bergmans et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. and Bergmans et al. by transferring information through interconnections formed passing through the layer as taught by Stein to prevent defects (col. 1, lines 22-48).

Findler et al. in view of Bergmans et al. do not disclose stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm².

Hori et al. disclose a method of lithographic pattern generation where an array of exposure cells is provided on a substrate, wherein the exposure cells expose separate areas of a surface to be exposed; and providing at least one stress-controlled dielectric layer on the substrate (col. 1, lines 9-13; col. 4, lines 5-59). Hori et al. further disclose the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm² (col. 8, lines 32-59). Hori et al. also disclose the stress as tensile (col. 8, lines 32-59).

Since Findler et al., Bergmans et al. and Hori et al. are both from the same field of endeavor, a method of lithographic pattern generation, the purpose disclosed by Hori et al. would have been recognized in the pertinent art of Findler et al. and Bergmans et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. and Bergmans et al. by the stress of the stress-controlled dielectric layer is less than about 8×10^8 dynes/cm² as taught by Hori et al. to increase density and stress stability (col. 4, lines 5-8).

Findler et al. in view of Bergmans et al. do not disclose the integrated circuit being able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

Shimizu et al. disclose a method of making an integrated circuit where a substrate (1) has a principal surface; and forming circuit devices/circuitry/active devices (4) on the principal surface (col. 1, lines 29-44). Shimizu et al. further disclose the integrated circuit being able to be thinned to about 25 microns throughout a full extent thereof while retaining its structural integrity (col. 1, lines 45-56).

Since Findler et al., Bergmans et al. and Shimizu et al. are both from the same field of endeavor, a method of making an integrated circuit, the purpose disclosed by Shimizu et al. would have been recognized in the pertinent art of Findler et al. and Bergmans et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. and Bergmans et al. by the integrated circuit being able to be thinned to about 25 microns throughout a full extent thereof while retaining its structural integrity as taught by to prevent defects (col. 1, lines 38-44).

Claims 449, 450, 454, 455, 472, 473, 477, 478, 482 and 483 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findler et al. in view of Rubinstein et al. (5,227,959).

Findler et al. disclose the subject matter claimed above except forming at least one flexible integrated circuit.

Referring to claims 449, 450, 454, 455, 472, 473, 477, 478, 482 and 483, Rubinstein et al. disclose a method of making integrated circuit where a flexible circuit (36) is formed over a substrate (10) (col. 4, lines 53-65).

Since Findler et al. and Rubinstein et al. are both from the same field of endeavor, a method of making integrated circuit, the purpose disclosed by Rubinstein et al. would have been recognized in the pertinent art of Findler et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. by forming at least one flexible integrated circuit as taught by Rubinstein et al. to reduce cross talk by controlling impedance (col. 3, lines 58-62; col. 6, lines 6-8).

Claims 459, 460, 463 and 464 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findler et al. in view of Stein as applied to claims 179 and 189 above, and further in view of Rubinstein et al.

Findler et al. in view of Stein disclose the subject matter claimed above expect forming at least one flexible integrated circuit.

Referring to claims 449, 450, 454, 455, 472, 473, 477, 478, 482 and 483, Rubinstein et al. disclose a method of making integrated circuit where a flexible circuit (36) is formed over a substrate (10) (col. 4, lines 53-65).

Since Findler et al. and Rubinstein et al. are both from the same field of endeavor, a method of making integrated circuit, the purpose disclosed by Rubinstein et al. would have been recognized in the pertinent art of Findler et al. Therefore, it would

Art Unit: 2822

have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. by forming at least one flexible integrated circuit as taught by Rubinstein et al. to reduce cross talk by controlling impedance (col. 3, lines 58-62; col. 6, lines 6-8).

Claims 467 and 468 are rejected under 35 U.S.C. 103(a) as being unpatentable over Findler et al. in view of Bergmans et al. as applied to claims 179 and 189 above, and further in view of Rubinstein et al.

Findler et al. in view of Bergmans et al. disclose the subject matter claimed above expect forming at least one flexible integrated circuit.

Referring to claims 467 and 468, Rubinstein et al. disclose a method of making integrated circuit where a flexible circuit (36) is formed over a substrate (10) (col. 4, lines 53-65).

Since Findler et al. and Rubinstein et al. are both from the same field of endeavor, a method of making integrated circuit, the purpose disclosed by Rubinstein et al. would have been recognized in the pertinent art of Findler et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Findler et al. by forming at least one flexible integrated circuit as taught by Rubinstein et al. to reduce cross talk by controlling impedance (col. 3, lines 58-62; col. 6, lines 6-8).

Art Unit: 2822

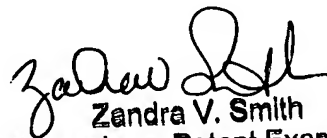
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PEP
16 June 2006


Zandra V. Smith
Supervisory Patent Examiner
21 June 2006

Continuation of Disposition of Claims: Claims pending in the application are 156-291,394-399,409-424,448-455,457,460,462-464,466-468,470-485 and 523-530.